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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
KIM, DAVID S	

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

BV

Office Action Summary	Application No.	Applicant(s)	
	10/780,718	AKITA ET AL.	
	Examiner	Art Unit	
	David S. Kim	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement filed on 19 February 2004 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but all of the information referred to therein has not been considered. In particular, there was no copy of the Japanese Patent Laid-Open Publication No. 57-37941.

Drawings

2. Applicant's response to the objection to the drawings in the previous Office Action (mailed on 09 February 2007) is noted and appreciated. Replacement drawings for Figs. 6-9 were received on 23 May 2007. However, these drawings are disapproved. These replacement drawings for Figs. 6-9 include a ***bidirectional*** link between clock selecting unit 93 and evaluating unit 84 and digital filter 82. However, Applicant's disclosure may only support a ***unidirectional*** link from clock selecting unit 93 to evaluating unit 84 and to digital filter 82.

In original independent claims 1 and 10, notice the following limitations:

(claim 1) "an electrical signal receiving unit...converting the electrical signal into a binary optical digital signal ***synchronized with the clock supplied from the clock supplying unit***" (emphasis Examiner's) and

(claim 10) "converting a binary optical digital signal input from the optical data transmission system into a multi-level electrical analog signal ***synchronized with the recovered clock***" and

"causing a multi-level electrical analog signal input from the electrical data transmission system to ***synchronize with the recovered clock***" (emphasis Examiner's).

The emphasized limitations suggest that Figs. 6-9 should show "electrical signal receiving unit" 80 with some input from "clock selecting unit" 93, but not an input to "clock selecting unit" 93 from evaluating unit 84 or from digital filter 82. Otherwise, the drawings include new subject matter that is not supported by Applicant's original disclosure. As a remedy, Examiner respectfully suggests drawing

amendments that reflect the end of Applicant's paragraph [0044], which notes that the "processes by the digital filter 82 and the evaluating unit 84 are basically performed in accordance with the clock output from the clock selecting unit 93". That is, Examiner respectfully suggests a ***unidirectional*** link from clock selecting unit 93 to evaluating unit 84 and to digital filter 82.

3. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the

examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Nakane as primary reference

6. **Claims 1-3** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakane (JP 05284192 A, machine-translated version).

Regarding claim 1, Nakane discloses:

An optical/electrical converting device for connecting an optical data transmission system (left side of Drawing 1 is optical), which includes a plurality of apparatuses performing data communication by an optical signal, and an electrical data transmission system (right side of Drawing 1 is electrical), which includes a plurality of apparatuses performing data communication by an electrical signal, and performing data communication between the optical data transmission system and the electrical data transmission system, the device comprising:

a clock supplying unit for supplying a clock (clock selected by clock selection circuitry 124 in Drawing 1) synchronized with a selected (clock selection circuitry 124 in Drawing 1) reference clock, the selection being between a first reference clock from the optical data transmission system and a second reference clock from the electrical data system (paragraphs [0004] and [0014] imply one clock from the optical side and another clock from the electrical side), wherein the selection is based on which of the optical data transmission system and the electrical data transmission system includes a designated master apparatus (selection is based on the host side in paragraph [0014] being in the optical side or in the electrical side);

an electrical signal transmitting unit (components 101 to 106) for receiving an optical digital signal from the optical data transmission system, converting (102) the optical signal into a multi-level electrical signal (bipolar signals on 106), and outputting the electrical signal to the electrical data transmission system (output on 106); and

an electrical signal receiving unit (components 107 to 112) for receiving a multi-level electrical analog signal from the electrical data transmission system, converting (111) the electrical signal into an

optical digital signal (unipolar signals on 112), and outputting the optical signal to the optical data transmission system (output on 112).

Nakane does not expressly disclose:

converting the optical signal into a multi-level electrical signal ***synchronized with the clock supplied from the clock supplying unit***; and

converting the electrical signal into an optical digital signal ***synchronized with the clock supplied from the clock supplying unit***.

However, these limitations are suggested. Notice the electrical signal that is retimed/synchronized through 104 (abstract) and the optical signal that is retimed/synchronized through 110 (abstract). These instances of retiming/synchronization suggest at least one clock to which these signals are retimed/synchronized. Also, notice that Nakane discusses the synchronization of a chosen clock of either the electrical system or the optical system ("one side" in paragraph [0005], "the clock of the side which should synchronize" in paragraph [0015]). This synchronization also suggests another clock to which this chosen clock should synchronize. At the time the invention was made, it would have been obvious to one of ordinary skill in the art to retime/synchronize all of the signals/clocks to the clock supplied from the clock supplying unit. One of ordinary skill in the art would have been motivated to do this to maintain signal and system synchronization between the electrical and optical sides of the apparatus. That is, notice that the apparatus of Nakane is primarily characterized as "media-conversion equipment" (Nakane, paragraph [0001]). As a primary function is simple media-conversion between an electrical medium to an optical medium, one would generally desire to maintain the integrity of characteristics of the signals that are switching between media, including characteristics of synchronization and timing. Synchronization and (re)timing according to one clock provides such maintenance of signal integrity.

Regarding claim 2, Nakane discloses:

The optical/electrical converting device according to claim 1, wherein

the clock supplying unit includes:

a first clock recovery unit (103) for recovering the first reference clock based on an optical signal input from the optical data transmission system;

a second clock recovery unit (109) for recovering the second reference clock based on an electrical signal input from the electrical data transmission system; and

a clock selecting unit (124) for selecting the first reference clock recovered by the first clock recovery unit if the master apparatus (host side in paragraph [0014] being in optical side) generating the first reference clock is included in the optical data transmission system, and selecting the second reference clock recovered by the second clock recovery unit if the master apparatus generating the second reference clock is included in the electrical data transmission system (host side in paragraph [0014] being in electrical side), and

the electrical signal transmitting unit converts the optical signal input from the optical data transmission system into an electrical signal synchronized with the reference clock selected by the clock selecting unit (see synchronization/timing argument in the treatment of claim 1 above).

Regarding claim 3, Nakane discloses:

The optical/electrical converting device according to claim 1, wherein

the clock supplying unit includes:

a first clock recovery unit (103) for recovering the first reference clock based on an optical signal input from the optical data transmission system;

a second clock recovery unit (109) for recovering the second reference clock based on an electrical signal input from the electrical data transmission system; and

a clock selecting unit (124) for selecting the first reference clock recovered by the first clock recovery unit if the master apparatus (host side in paragraph [0014] being in optical side) generating the first reference clock is included in the optical data transmission system, and selecting the second reference clock recovered by the second clock recovery unit if the master apparatus generating the second reference clock is included in the electrical data transmission system (host side in paragraph [0014] being in electrical side), and

the electrical signal transmitting unit converts the optical signal input from the optical data transmission system into an electrical signal, and replaces the clock recovered by the first clock recovery unit with the reference clock selected by the clock selecting unit (according to the synchronization/timing argument in the treatment of claim 1 above, synchronizing/(re)timing the signals and systems to one clock would obviously replace other unsynchronized clocks, such as the clock recovered by the first clock recovery unit) while maintaining synchronization (according to the synchronization/timing argument in the treatment of claim 1 above, maintaining synchronization is obviously desirable to maintain the integrity of characteristics of the signals that are switching between media).

7. **Claims 4-5** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakane as applied to the claims above, and further in view of Ono et al. (U.S. Patent Application Publication No. US 2002/0168137 A1, hereinafter "Ono").

Regarding claim 4, Nakane discloses:

The optical/electrical converting device according to claim 1, wherein

the clock supplying unit includes:

a clock recovery unit (109) for recovering the second reference clock based on an electrical signal input from the electrical data transmission system; and

a clock selecting unit (124) for selecting the second clock recovered by the clock recovery unit if the master apparatus generating the second reference clock is included in the electrical data transmission system (host side in paragraph [0014] being in electrical side), and

the electrical signal transmitting unit converts an optical signal input from the optical data transmission system into an electrical signal synchronized with the reference clock selected by the clock selecting unit (see synchronization/timing argument in the treatment of claim 1 above).

Nakane does not expressly disclose:

the clock selecting unit (124) for selecting the first reference clock input from an apparatus, whose clock synchronization is already established, included in the optical data transmission system, if the master apparatus generating the first reference clock is included in the optical data transmission system.

However, this limitation appears to read on an externally provided clock from the optical data transmission system, which is known in the art, as shown by Ono (Fig. 12, external clock signal). At the time the invention was made, it would have been obvious to one of ordinary skill in the art to select a clock input from any number of source locations of a desired clock signal, including an externally provided clock from the optical data transmission system, as shown by Ono (Fig. 12, various clock sources). One of ordinary skill in the art would have been motivated to do this since Ono shows that the location of the source of a chosen reference clock can be variable and not limited to particular locations (Ono, notice the clock selection from local extraction parts, a local generating part, or an external clock signal), increasing flexibility in design and implementation.

Regarding claim 5, claim 5 is a claim that corresponds largely to claim 1. Therefore, the recited limitations in claim 1 read on the corresponding limitations in claim 5. Claim 5 also includes limitations absent from claim 1. Nakane in view of Ono also discloses these limitations:

wherein the clock supplying unit includes a clock recovery unit (Nakane, 109) for recovering a clock based on an electrical signal input from the electrical data transmission system;

a clock generating unit (Ono, 128-c in Fig. 12) for generating the first reference clock to which the master apparatus is locked; and

a clock selecting unit (Nakane, 124) for selecting the first reference clock generated by the clock generating unit if the master apparatus locked by the first reference clock is included in the optical data transmission system (host side in paragraph [0014] being in optical side), and selecting the second reference clock recovered by the clock recovery unit if the master apparatus generating the second reference clock is included in the electrical data transmission system (host side in paragraph [0014] being in electrical side), and

wherein the electrical signal transmitting unit converts an optical signal input from the optical data transmission system into an electrical signal synchronized with the reference clock selected by the clock selecting unit (see synchronization/timing argument in the treatment of claim 1 above).

8. **Claims 6-9** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakane in view of Ono as applied to the claims above, and further in view of Katta et al. (WO 02/30079, hereinafter "Katta", references are made to the English translation of Katta in corresponding U.S. Patent No. 7,133,936 B2).

Regarding claims 6-9, Nakane in view of Ono does not expressly disclose:

wherein the electrical signal receiving unit

sends an electrical signal input from the electrical data transmission system to the electrical signal transmitting unit until completion of initialization of the apparatuses included in the electrical data transmission system, and

after completion of the initialization of the apparatuses included in the electrical data transmission system, converts an electrical signal input from the electrical data transmission system into an optical signal synchronized with the reference clock selected by the clock selecting unit, and outputs the optical signal to the optical data transmission system.

However, Katta teaches these limitations as part of an initialization process of a ring network (Katta, col. 10, l. 59 – col. 11, l. 37). At the time the invention was made, it would have been obvious to one of ordinary skill in the art to implement a ring network and a corresponding initialization process in the apparatus of Nakane in view of Ono. One of ordinary skill in the art would have been motivated to do this since Nakane in view of Ono is relatively silent about the details of the system that is connected to its electrical side, and the teachings of Katta would suitably speak into this silence. That is, a ring configuration is an extremely common way to configure a system on the electrical side of Nakane in view of Ono. Additionally, as Katta teaches a corresponding initialization process for a ring system, it follows that an obvious version of the system of Nakane in view of Ono and Katta would include some kind of initialization process so that the system would be ready to perform data communication (Katta, col. 2, l. 6-8).

9. **Claim 10** is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakane in view of Katta. This rejection relies on the combination of Nakane and Katta as combined above in the treatment of claims 6-9. However, this rejection does not rely on the referenced teachings of Ono.

Regarding claim 10, Nakane in view of Katta discloses:

An optical/electrical converting method for connecting an optical data transmission system (Nakane, left side of Drawing 1 is optical), which includes a plurality of apparatuses performing data communication by an optical signal, and an electrical data transmission system (Nakane, right side of Drawing 1 is electrical), which includes a plurality of apparatuses performing data communication by an electrical signal, and performing data communication between the optical data transmission system and the electrical data transmission system, comprising the steps of:

recovering a first reference clock (Nakane, 103 and 124) based on an optical signal input from the optical data transmission system;

recovering a second reference clock (Nakane, 109 and 124) based on an electrical signal input from the electrical data transmission system;

supplying a clock (Nakane, clock selected by clock selection circuitry 124 in Drawing 1) synchronized with a selected (Nakane, clock selection circuitry 124 in Drawing 1) reference clock, the selection being between the first reference clock recovered from the optical data transmission system, and the second reference clock recovered from the electrical data transmission system (Nakane, paragraphs [0004] and [0014] imply one clock from the optical side and another clock from the electrical side), wherein the selection is determined based on which of the optical data transmission system and the electrical data transmission system includes a designated master apparatus (Nakane, selection is based on the host side in paragraph [0014] being in the optical side or in the electrical side);

converting (Nakane, components 101 to 106) an optical digital signal input from the optical data transmission system into a multi-level electrical signal synchronized with the supplied clock (Nakane, see synchronization/timing argument in the treatment of claim 1 above), and outputting the electrical signal to the electrical data transmission system (Nakane, output on 106);

synchronizing a multi-level electrical analog signal received from the electrical data transmission system with the supplied clock (Nakane, see synchronization/timing argument in the treatment of claim 1 above), and outputting the electrical signal to the electrical data transmission system until completion of

initialization (Katta, col. 10, l. 59 – col. 11, l. 37) of the apparatuses included in the electrical data transmission system; and

converting (Nakane, components 107 to 112) a multi-level electrical signal input from the electrical data transmission system into an optical digital signal synchronized with the recovered clock (Nakane, see synchronization/timing argument in the treatment of claim 1 above), and outputting the optical signal to the optical data transmission system after completion (Katta, col. 10, l. 59-63, col. 11, l. 23-29) of the initialization of the apparatuses included in the electrical data transmission system.

Response to Arguments

10. Applicant's arguments filed on 23 May 2007 have been fully considered but they are not persuasive. Applicant's arguments are based on the limitations introduced by Applicant's most recent amendment filed on 23 May 2007. In particular, notice the limitations of selection of a reference clock between a first reference clock and a second reference clock based on which of the optical data transmission system and the electrical data transmission system includes a designated master apparatus (see independent claims 1, 5, and 10). Applicant states that the prior art of record does not teach these limitations (REMARKS, p. 12, 1st full paragraph; p. 12, 2nd full paragraph; p. 12-13, bridging paragraph; p. 13, 1st full paragraph).

Examiner respectfully points to teachings from Nakane to show these limitations. Notice the selection of a reference clock (clock selection circuitry 124 in Drawing 1) between a first reference clock and a second reference clock (paragraphs [0004] and [0014] imply one clock from the optical side and another clock from the electrical side). Next, notice that this selection is based on which of the optical data transmission system and the electrical data transmission system includes a designated master apparatus (selection is based on the "host", synonymously known as a "master", side in paragraph [0014] being in the optical side or in the electrical side). Accordingly, Applicant's arguments are not persuasive.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Notice the English translation of Nakane by The McElroy Translation Company.

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David S. Kim whose telephone number is 571-272-3033. The examiner can normally be reached on Mon.-Fri. 9 AM to 5 PM (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth N. Vanderpuye can be reached on 571-272-3078. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DSK

KENNETH VANDERPUYE
SUPERVISORY PATENT EXAMINER

"REPLACEMENT SHEET"

Disapproved by DSK
11 AUGUST 2007

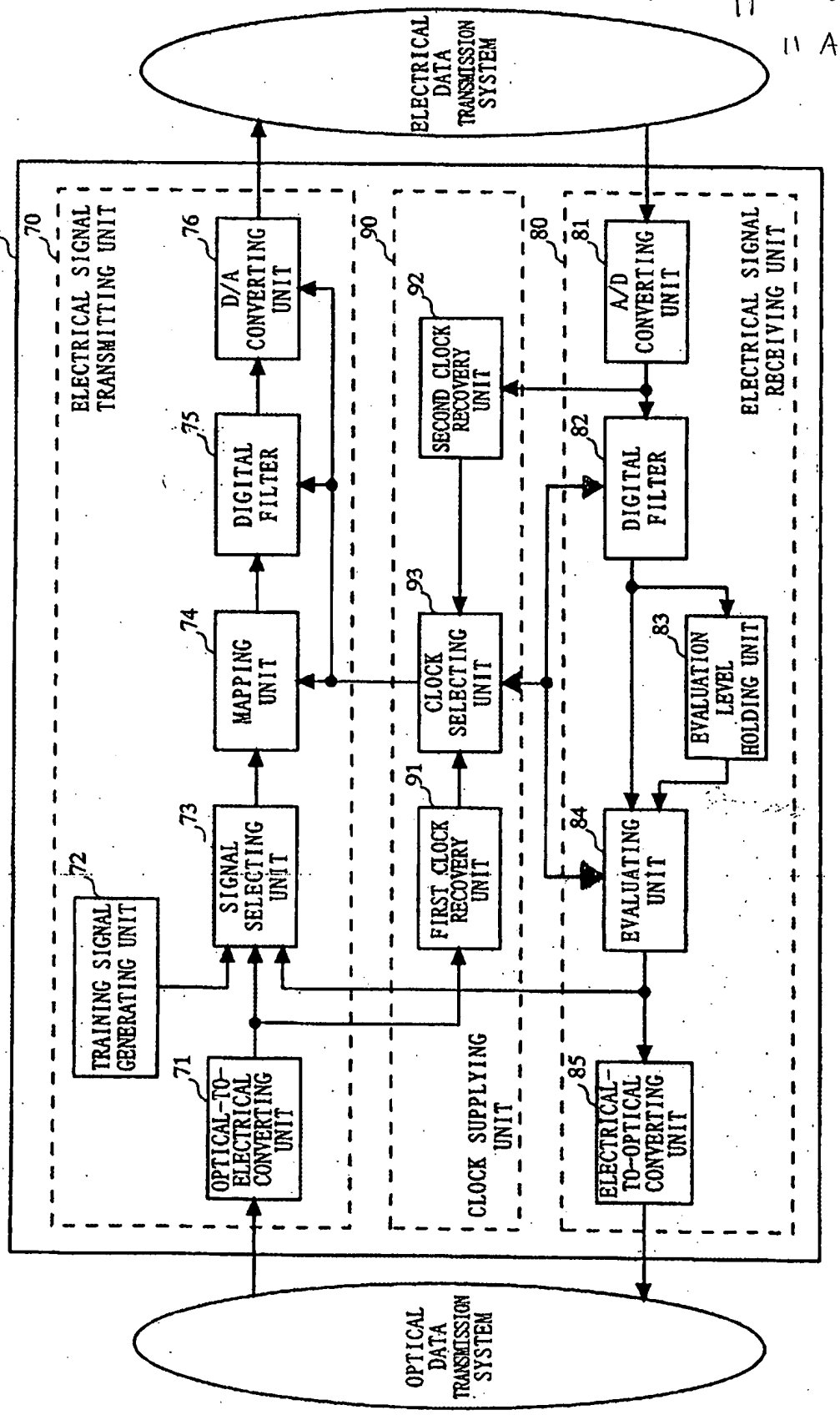
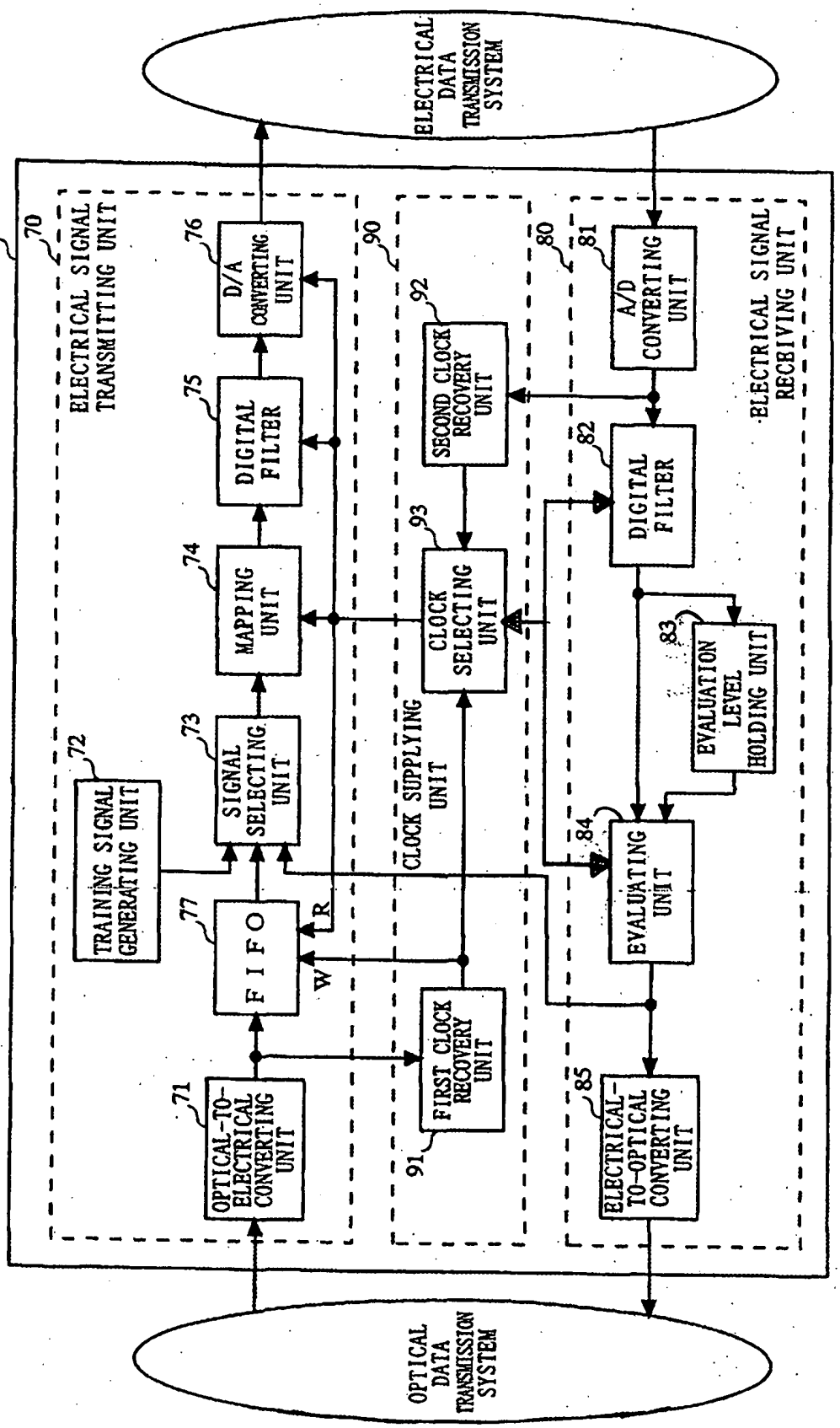


FIG. 6

"REPLACEMENT SHEET"

Disapproved by PSK
11 AUGUST 2007

FIG. 7



"REPLACEMENT SHEET"

DB approved by DSK
11 AUGUST 2001

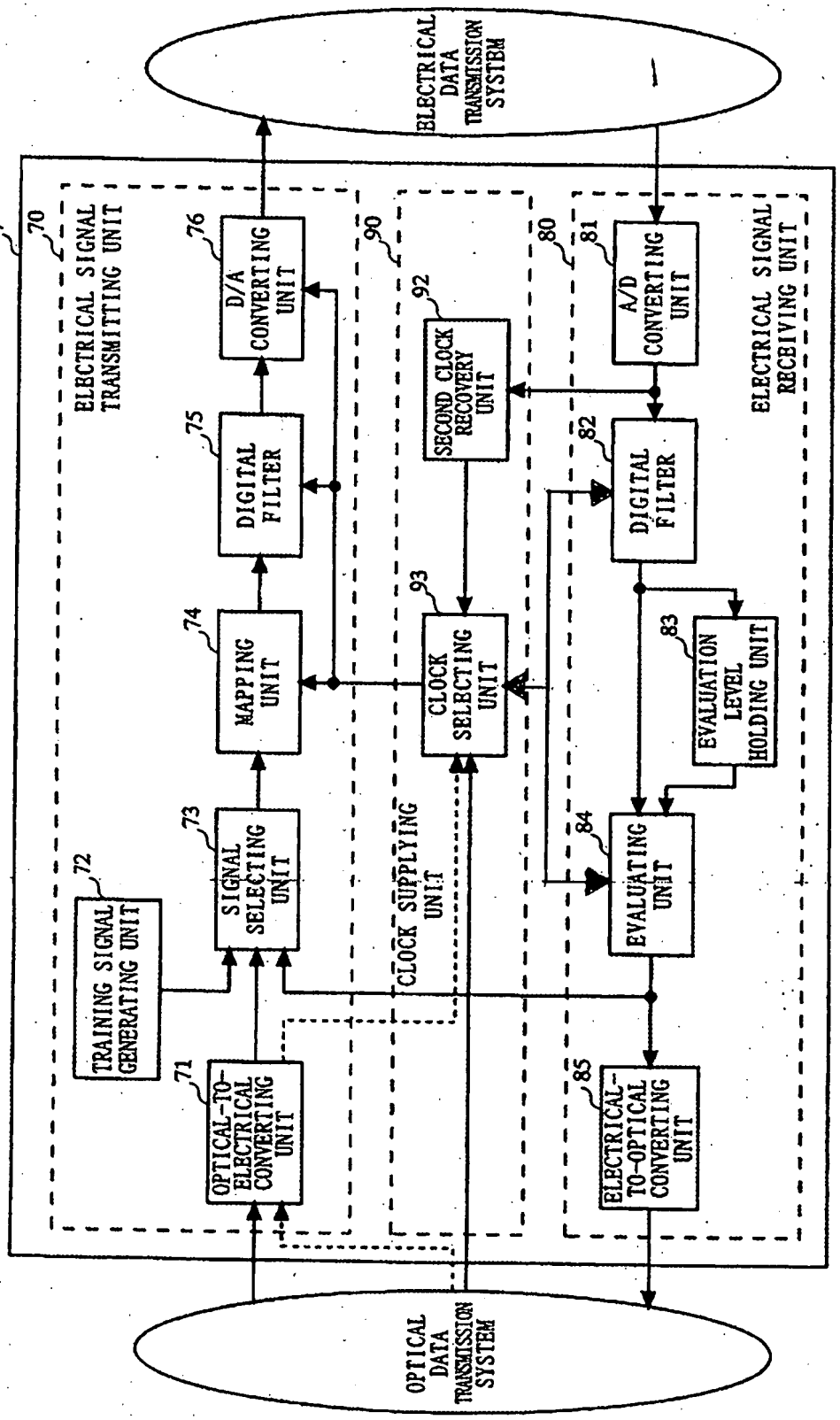


FIG. 8

"REPLACEMENT SHEET"

DBapproved by PSK
11 AUGUST 2007

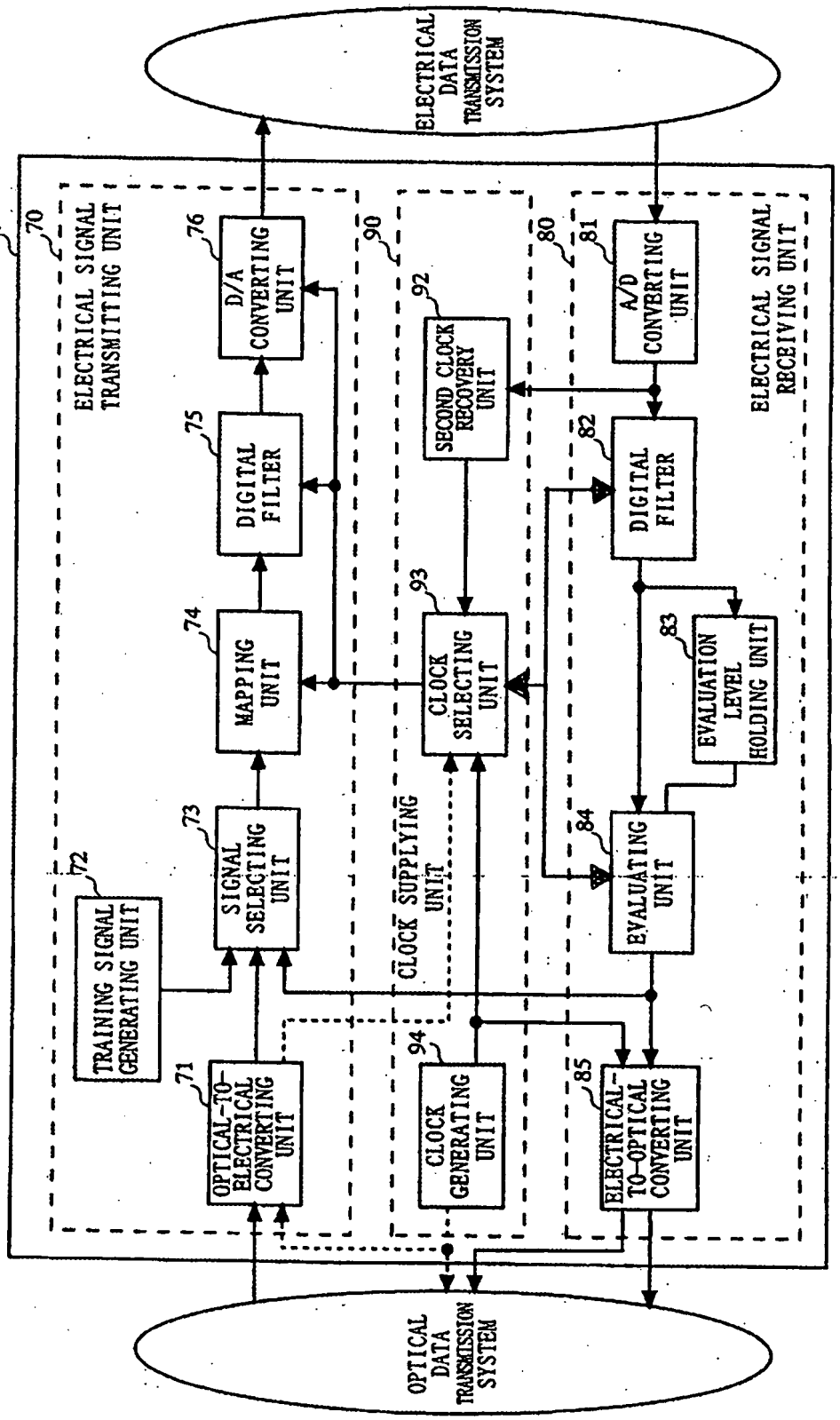


FIG. 9